IN THE SPECIFICATION

Please amend the paragraph starting on page 10, line 34 as follows:

--The request signals REQ1 through REQn transmitted by the respective masters 12-1 through 12-n are supplied to arbiter 11, and the grant signals GNT1 through GNTn are [[also]] supplied to the OR circuit 18. The OR circuit 18 obtains a logic sum of the grant signals GNT1 through GNTn ~~request signals REQ1 through REQn~~, and supplies its output to the counter 19. The counter 19 performs counting each time the signal from the OR circuit 18 is asserted. In other words, the OR circuit 18 counts up (or counts down) each time any one of the masters 12-1 through 12-n carries out a request operation and is granted the right to use the bus. If a 4-bit counter is used, for example, numbers are counted in an ascending order from 1, and the count returns to 1 when it reaches 16. Alternatively, numbers are counted in a descending order from 16, and the count returns to 16 when it reaches 1.--